S.E EXTC -(CBCS) (Sem III)

EDC - I

Q.P. Code: 25073

29 NOV 2017

Time: 3 Hours **Marks: 80**

N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three questions from the remaining five questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 Attempt any 5 questions **[20]**

(a) Explain various types of capacitors.
(b) Why should collector resistor R_C be as large as possible in the design of CE amplifier?
(c) Explain Zener as voltage regulator.
(d) State and explain Miller's Theorem.
(e) Draw and explain small signal model of a diode.
(f) Explain the hybrid pi model of BJT.

Q.2 (a) Explain the fabrication steps of passive elements. **[5]**
(b) Explain concept of zero temperature drift in JFET. **[5]**
(c) Design an L section *LC* filter with full wave rectifier to meet the following specifications: The DC output voltage $V_{DC} = 220$ V deliver $I_L = (70 \pm 20)$ mA to the resistive load and the required ripple factor is 0.04. **[10]**

Q.3 (a) Draw small signal hybrid parameter equivalent circuit for CE amplifier and define the same. What are the advantages of h parameters? **[10]**
(b) Determine I_{DQ}, V_{GSQ}, V_{DSQ} if $I_{DSS} = 9$ mA and $V_p = -3$ V for the circuit given in Fig. 3(b). **[10]**

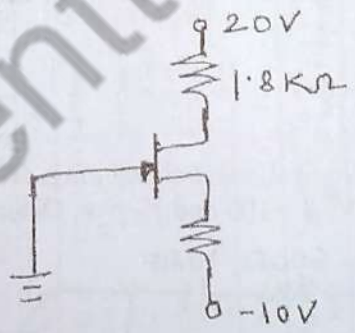

Fig. 3(b)

Q.4 (a) Design the resistors of a single stage CS amplifier for audio frequency with BFW11 with $I_{DS} = (3.3 \pm 0.6)$ mA and $|A_v| = 12$. **[10]**

(b) For the circuit shown below in Fig.4(b), the transistor parameters are $V_{BE(on)} = 0.7$ V, $\beta = 200$ and $V_A = \infty$. **[10]**
i) Derive the expression for lower cut-off frequency (or time constant) due to input coupling capacitor.
ii) Determine lower cut-off frequency and midband voltage gain.

TURN OVER

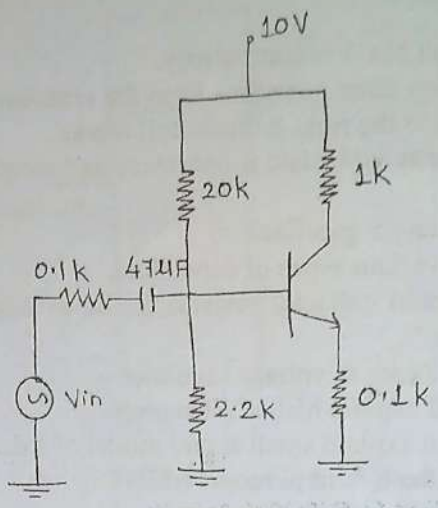

Fig. 4(b)

Q.5 (a) For the circuit using JFET as shown in Fig. 5(a), if I_{DSS} = 6 mA, V_p = -6 V, rd= ∞, C_{gd}= 4 pF, C_{gs}= 6 pF, C_{ds}= 1 pF, Determine i) V_{GSQ}, ii) I_{DQ}, iii) gmo, and iv) gm. [10

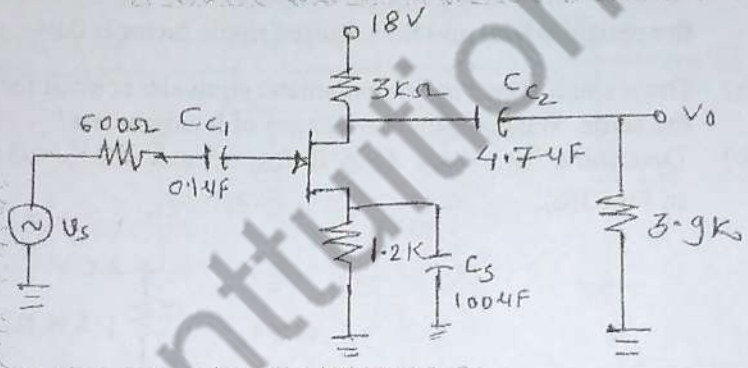

Fig. 5(a)

(b) For the circuit shown below in Fig. 5(b), the transistor parameters are V_{BE} [1
$_{(on)}$ = 0.7 V, β = 100 and V_A = ∞. Determine Z_i, Z_o and A_V.

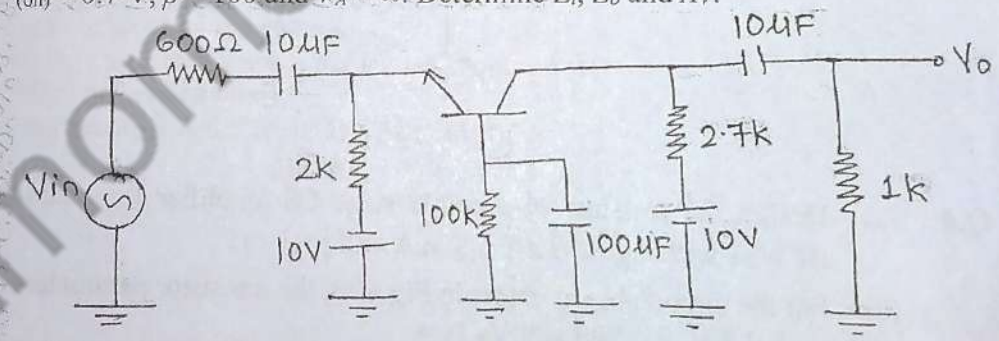

Fig. 5(b)

Q.6 Short notes on: (Attempt any four)

(a) High frequency π equivalent model of common emitter BJT.
(b) Stability factors of various biasing techniques of BJT.
(c) Comparison of BJT CE and JFET CS amplifier.
(d) Different types of filters.
(e) JFET parameters.

Transistor type	P_{tot} @ 25°C Watts	I_{Cmax} @ 25°C Amps	V_{CE} (sat) volts d.c.	V_{CBO} volts d.c.	V_{CEO} (Sus) volts d.c.	V_{CER} (Sus) volts d.c.	V_{CEX} volts d.c.	V_{EBO} volts d.c.	T_j max °C	D.C. current gain min.	typ.	max.	Small Signal h_{fe} min.	typ.	max.	f_h	V_{BE} max.	θ_{j-c} °C/W	Derate above 25°C m W/°C
2N 3055	115·5	15·0	1·1	100	60	70	90	7	200	20	50	70	15	50	120	1·8	1·5	0·7	
ECN 055	50·0	5·0	1·0	60	50	55	60	5	200	25	50	100	25	75	125	1·5	3·5	0·4	
SCN 149	30·0	4·0	1·0	50	40	—	—	8	150	30	50	110	33	60	115	1·2	4·0	0·3	
ECN 100	5·0	0·7	0·6	70	60	65	—	6	200	50	90	280	50	90	280	0·9	15	0·05	
BC147A	0·25	0·1	0·25	50	45	50	—	6	125	115	180	220	125	270	260	0·9	—	—	
2N 525(PNP)	0·225	0·5	0·25	35	30	—	—	—	160	35	—	65	—	45	—	—	—	—	
BC147B	0·25	0·1	0·25	50	45	50	—	6	125	200	290	450	240	330	500	0·9	—	—	

BFW 11—JFET MUTUAL CHARACTERISTICS

Transistor type	hfe	hoe	θja
BC 147A	2·7 K Ω	18μ Ʊ	1·5 × 10⁻⁴	0·4°C/mW
2N 525 (PNP)	1·8 K Ω	25μ Ʊ	3·2 × 10⁻⁴	—
BC 147B	4·5 K Ω	30μ Ʊ	2 × 10⁻⁴	0·4°C/mW
ECN 100	500 Ω	—	—	—
ECN 149	250 Ω	—	—	—
ECN 055	100 Ω	—	—	—
2N 3055	25 Ω	—	—	—

N-Channel JFET Type	V_{DS} max. Volts	V_{DS} max. Volts	V_{GS} max. Volts	P_T max. @25°C	T_j max.	I_{DSS}	g_{os} (typical)	$-V_P$ Volts	r_d	Derate above 25°C
LN3822	50	50	50	300 mW	175°C	2 mA	3000 μ Ʊ	6	50 KΩ	2 mW/°C	0·59°C/mW
BFW 11 (typical)	30	30	30	300 mW	200°C	7 mA	5600 μ Ʊ	2·5	50 KΩ	—	0·59° C/mW