B.E. EXTC SEM III
CBCGS
Choice Based.
DSD.

07 DEC 2017

Q.P. Code: 27581

N.B.:
1. Question No. 1 is compulsory.
2. Attempt any three questions out of remaining five questions.
3. Figures to the right indicate full marks.
4. Assume suitable data if required and mention it in answer sheet.

Q1. Solve following (20 Marks)

a) Explain the following decimals in gray code form
   1. $(42)_{10}$ 2. $(17)_{10}$

b) Explain Mealy machine and Moore machine

c) Design a full adder using 3:8 Decoder

d) Convert JK flip flop to T flip flop.

Q2. a) Prove that NAND and NOR gates are Universal gates. (10 Marks)

b) Implement the following Boolean function using 8:1 multiplexer. (10 Marks)
$F(A,B,C,D)=\sum M(0,1,4,5,6,8,10,12,13)$

Q3. a) Explain the Johnson's Counter. Design for initial state 0110. From initial state explain and draw all possible states. (10 Marks)

b) Minimize the following expression using Quine Mc-cluskey technique. (10 Marks)
$F(A,B,C,D)=\sum M(0,1,2,3,5,7,9,11)$

Q4. a) Design a 2 bit comparator and implement using logic gates (10 Marks)

b) Using Boolean Algebra Prove the following
1. $AB+BC+\overline{A}C=AB+\overline{A}C$
2. $[(C+\overline{C}D)(C+\overline{C}\,\overline{D}\,][AB+\overline{A}\,\overline{B}+(A \text{ XOR } B)]=C$ (10 Marks)

Q5. a) Explain the working of 3 bit asynchronous counter with proper timing diagram (10 Marks)

b) What is shift register? Explain any one type of shift register. Give its applications. (10 Marks)

(20 Marks)

Q6.
a) VHDL Code for Full Subtractor
b) Explain CPLD and FPGA
c) Explain SRAM and DRAM.
d) Compare TTL and CMOS logic families

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