SE EXTC Sem-III Choice based

DSD

Q. P. Code : 39546

(3 Hours) 80 Marks

22 MAY 2018

N.B.: (1) Question No. **1 is compulsory.**

(2) Solve any **three questions** from the **remaining five**

(3) Figures to the right indicate full marks

(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 a) If $F(A,B,C)=\sum m(0,3,5,7)$ with its truth table and express F in SOP and POS form [20]

b) Compare TTL and CMOS Logic families

c) Perform the following operation using 2's compliment

i) $(7)_{10}-(15)_{10}$

ii) $(50)_{10}-(2A)_{16}$

Comment on results of (i) and (ii)

d) Compare SRAM with DRAM

Q.2 a) Implement following Boolean function using 8:1 multiplexer [10]

$F(A,B,C,D) = \overline{A}\,B\,\overline{D} + A\,C\,D + \overline{B}\,C\,D + \overline{A}\,\overline{C}\,D$

b) Design 3 bit Binary to Gray code Converter [10]

Q.3 a) What are shift registers? How are they classified? Explain working of any one type of shift register. [10]

b) Write VHDL code for 3 bit up counter. [10]

Q.4 a) Explain Master slave JK Flip flop [5]

b). Convert T flip flop to D flip flop. [5]

c) Minimize the following expression using Quine McClusky Technique [10]

$F(A,B,C,D)=\sum m(1,3,7,9,10,11,13,15)$

Q.5 a) State and prove Demorgan's theorem [5]

b) b) Convert $(532.125)_8$ into decimal, binary and hexadecimal. [5]

c) Explain Full Adder circuit using PLA having three inputs, 8 product terms and two outputs. [10]

Q.6 a) Prove that NAND and NOR gates are universal gates [10]

b) Draw and explain 3 bit asynchronous binary counter using positive edge triggered JK flip flop. Draw the waveforms. [10]

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