



# Digital Logic Design and Analysis

JUN 19

Computer Engineering (Semester 3)

**Total marks: 80**

**Total time: 3 Hours**

## INSTRUCTIONS

(1) Question 1 is compulsory.

(2) Attempt any **three** from the remaining questions.

(3) Draw neat diagrams wherever necessary.

- 1.a.** Convert  $(451.43)_{10}$  into octal, binary and hexadecimal and base 7. (4 marks)
- 1.b.** Subtract using 1's and 2's complement method  $(73)_{10} - (49)_{10}$ . (4 marks)
- 1.c** Perform  $(52)_{10} - (68)_{10}$  in BCD using 9's complement. (4 marks)
- 1.d.** State De Morgan's theorem. Prove OR-AND configuration is equivalent to NOR-NOR configuration. (4 marks)
- 1.e.** Encode the data bits 111010001 using Hamming code. (4 marks)
- 1.f.** Explain SOP and POS and solve the following using K-Map  
 $F(A,B,C,D) = \pi M(1,3,5,6,7,10,11) + d(2,4)$ . (4 marks)
- 1.g.** Explain lockout condition. How can it be avoided. (4 marks)
- 2.a.** Reduce equation using Quine McCluskey method and realize circuit using basic gates.  
 $F(A,B,C,D) = \sum m(1,5,6,12,13,14) + d(2,4)$  (10 marks)
- 2.b.** Design 4-bit BCD subtractor using IC 7483. (10 marks)
- 3.a.** Implement the following using only one 8:1 Mux.  
 $F(A,B,C,D) = \sum m(0,2,4,6,8,10,12,14)$  (5 marks)
- 3.b.** Design a Full Subtractor using only NAND gates. (5 marks)
- 3.c.** Design a logic circuit to convert 4-bit gray code to its corresponding BCD code. (10 marks)
- 4.a.** Compare different logic families with respect to fan in, fan out, speed, Propagation delay and power dissipation. (5 marks)
- 4.b.** Implement 3 bit binary to gray code converter using Decoder. (5 marks)
- 4.c.** Explain 4 bit bidirectional shift register. (10 marks)



- 5.a.** Design mod 13 synchronous counter using T flipflop. (10 marks)  
**5.b.** Convert SR flipflop to JK flipflop and D flipflop. (10 marks)

**Write short note on (any four)**

- 6.a.** ALU (5 marks)  
**6.b.** 3 bit Up/Down Asynchronous Counter (5 marks)  
**6.c.** Octal to Binary Encoder (5 marks)  
**6.d.** 4-bit Universal shift register (5 marks)  
**6.e.** VHDL (5 marks)