LAST MOMENT TUITIONS

Computer Organization and Architecture

DECEMBER 17

Computer Engineering (Semester 4)

Total marks: 80
Total time: 3 Hours

INSTRUCTIONS
(1) Question 1 is compulsory.
*(2) Attempt any **three** from the remaining questions.*
(3) Draw neat diagrams wherever necessary.

Q1 Solve any Four

1.a List different memory organization characteristics. (5 marks)

1.b What is IO buffering? (5 marks)

1.c In Floating point representation how to identify sign of exponent? (5 marks)

1.d What is virtual memory? (5 marks)

1.e What is TLB? (5 marks)

2.A. i) Draw the flow chart for Booth's Algorithm for two's complement multiplication. (4 marks)

ii) Using Booth's algorithm Multiply 14 times - 5. (6 marks)

2.B Describe hard-wire control unit and specify its advantages. (10 marks)

3.A Compare interrupt driven I/o and DMA. (10 marks)

3.B Calculate the hit and miss using various page replacement policies LRU, OPT, FIFO for following sequence (page frame size 3) 4,7,3,0,1,7,3,8,5,4,5,3,4,7,534 state which one is best for above example?

(10 marks)

4.A Explain set associative and associative cache mapping techniques. (10 marks)

4.B Explain Flynn's classification. (10 marks)

5.A Explain six stage instruction pipeline with suitable diagram. (10 marks)

5.B. i) Differentiate between RISC and CISC (5 marks)

ii) Differentiate between SRAM and DRAM. (5 marks)

6.A Explain different pipe lining hazards (10 marks)

6.B Explain in brief cache coherency problem. (10 marks)